REMARKS/ARGUMENTS

The Office Action of August 12, 2008, has been carefully reviewed and these remarks are responsive thereto. Claims 1-25 remain pending in this application. Claims 1, 10, 13, 16, 23 and 25 have been amended. Reconsideration and allowance of the instant application are respectfully requested.

Rejections of Claims 1-8, 10, and 12 under 35 U.S.C. § 103

Claims 1- 8, 10 and 12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Harris et al. (Testing and Diagnosis of Interconnect Faults in Cluster-based FPGA Architectures, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume 21, Issue 11, November 2002, Pages 1337-1343) in view of Venkatesan (Modelling Feedback Control Adjustment to Control Output Product Quality, Proceedings of American Control Conference, May 2002, vol. 6, pages 5049-5053). Applicants respectively traverse. Applicants have made a broadening amendment to Claim 1 to correct a typographical error with respect to the antecedent basis of the term "*N*-bit input." In the original claim 1, the "input" to the "verifier" was incorrectly referred to as "the N-bit input" of "each configurable logic block of the second set." Claim 10 was amended for similar reasons.

Venkatesan is non-analogous art. To rely on a reference under 35 U.S.C. 103(a), the art must be analogous in which there must be some reason for one skilled in the art to combine the reference. See *MPEP* 2141.01(a). As the Supreme Court held in *KSR Int'l Co. v. Teleflex Inc*, "any need or problem known in the field of endeavor at the time of the invention and addressed by the [the reference] can provide a reason for combining the elements in the manner claimed." *KSR Int'l Co. v. Teleflex Inc.*, 127 S.Ct. 1727 (2007). The office action provides no rationale, no "need or problem," other than conclusory statements, as to why one skilled in the art would have combined the teachings of Venkatesan with teachings of Harris to arrive at Applicants' present claims. The Applicants' claims 1-8, 10 and 12 pertain to testing configurable logic blocks in an emulation system. Configurable logic blocks pertain to digital systems, such as in digital integrated circuits containing primitive logic elements operating in discrete states (1 and 0). Conversely, as Venkatesan states:

> This paper describes a method to model feedback control adjustment to control the quality of products at the output of a continuous process. The method takes into consideration situations in which the product quality mean is on target and not on target by assigning probabilities for the respective situations. . . . In making feedback control adjustments, it is probable that because of its automatic nature, deficiencies in the feedback control loop such as inexact feedback error and incomplete feedback compensation, the feedback control adjustment is incomplete. . . . A probability model for feedback control adjustment based on a simple probability test for feed back control adjustment indicates that the product quality mean is not on target by sounding process 'out of control' alarm signals. (Venkatesan ,Abstract,).

Venkatesan pertains to control theory. More specifically, Venkatesan discloses adjusting feedback compensation in a continuous, i.e., ***analog***, process for producing products, based on such things as probability models of the system. Venkatesan discloses nothing remotely relevant to Applicant's present claims or relevant to the field of endeavor of Applicants' claims, i.e., testing *digital* logic. The office action presents no evidence that one skilled in the art of Applicants' claimed subject matter would have knowledge of or understand the field of endeavor of Venkatesan's disclosed subject matter.

Harris is not combinable with Venkatsan. Even assuming, without admitting, that Venkatsan is analogous art, Venkatesan is technically not combinable with Harris. Harris pertains to testing faults in FPGAs containing primitive logic elements operating in discrete states (1 and 0). One skilled in the art of the technology disclosed in Harris would have no technical means for incorporating the teachings of a continuous, i.e., *analog*, feedback system as disclosed in Venkatesan with the *digital* primitive logic elements operating in discrete states. The office action presents no evidence on how one skilled in the art of Harris' subject matter could make such a combination possible. Indeed, to attempt to do so would appear to destroy the utility of both Harris and Venkatsan.

Harris and Venkatsan do not teach each and every limitation of claims 1-8, 10, and 12. Even assuming, without admitting, that Venkatsan is both analogous and technically combinable with Harris, the combination alleged by the office action does not teach each and every limitation in Applicants' rejected claims. Applicant's assert that the neither Venkatsan, nor Harris, teach the claim 1 features of:

wherein the verifier is configured to accept its own output and the multi-bit output of the group of configurable logic blocks as an input,

wherein, upon the output of the verifier being a failure indicator, the verifier is configured to maintain the failure indicator for the test.

The office action asserts that the Venkatesan abstract, quoted above, discloses this limitation. However, a plain reading of the abstract shows it discloses adjusting feedback compensation in a continuous, i.e. *analog*, process for producing products, based on such things as probability models of the system. The remainder of Venkatesan discloses similar subject matter as the abstract. The Applicants' can find nothing in Venkatesan remotely similar to the claimed language.

Because the combination of Venkatsan and Harris fail to teach or suggest each and every limitation which is contained in independent claim 1, because Venkatsan is not technically combinable with Harris, because Venkatsan in non-analogous art, and because none of the other cited art teach these limitations, Applicants' respectfully request withdrawal of the rejection. Claims 2-8, 10 and 12 are allowable for at least the same reasons as their respective base claim 1, and further in view of the additional features recited therein.

For example, the combination of Harris and Venkatsan fails to teach claim 2 reciting, "configuring the second set to be second testing circuitry; and operating the second set to test the first set." Harris discloses, as cited by the office action, "In order to guarantee testing of all tiles, the FPGA will be reconfigured to shift the BISTERs across the entire array as shown in Fig. 4. Over the course of several reconfigurations, all tiles will be tested by acting as a BUT in a BISTER." (Harris, p. 1338, col. 2, para. 3-4). This disclosure does not state that the "second set," that is tested by the "first set," is configured to have the "first set" be tested by the "second set."

As another example, the combination of Harris and Venkatsan fails to teach claim 6, reciting, "configuring a configurable logic block of the first set to determine whether the *N*-bit input generator outputs a predetermined value." Harris recites, "The TPG is a simply a counter which applies an exhaustive test sequence to the BUTs." Applying an "exhaustive test sequence" is not the same as determining whether the N-bit input generator outputs a predetermined value.

As further example, the combination of Harris and Venkatsan fails to teach claim 10, which states that the "verifier," "group," and "multi-bit" output have a specific number of bits relative to each other. Harris, as cited by the office action, only makes a non-specific statement that the number of tiles in a BISTER will depend on a number of tiles needed to implement the TPG and ORA logic. (Harris, p. 1338, col. 2, para. 3).

Rejections of Claims 13-17, and 23 under 35 U.S.C. § 103

Claims 13- 17 and 23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 5,036,473, hereinafter Butts, in view of U.S. Pat. No. 6,470,485, hereinafter Cote, and U.S. Pat. No. 5,745,372, hereinafter Fluegge. Applicants respectively traverse. Applicants' have amended claim 13 and claim 23 to a more preferred form without changing the scope of the claims. Claim 16 has been amended to correct a typographical error.

Butts, Cote and Fluegge do not teach each and every limitation of claims 13-17, and 23. Assuming, without admitting, that the combination of Butts, Cote and Fluegge is proper, the combination fails to teach or suggest each and every feature of Applicants' claim 13. The office action cites fig. 3 and column 5, lines 5-16 of Fluegge which states:

> "... a signal must go from ... one SECTOR to ... another SECTOR, ... the signal must traverse through a level zero wire, then to a level one wire, then to a level two wire, then to a level three wire, and then to a level four wire ... [o]nce the signal reaches the other SECTOR, it must reverse this route from the level four wire in that SECTOR, down to a level three wire, down to a level two wire, then down to a level one wire, and finally down to a level zero wire ...." (emphasis added)

The office action alleges that Fluegge describes the Applicants' claimed feature, "configuring a second routing portion to map *N* inputs of the second routing portion to *N* outputs of the second routing portion in a second configuration inversely mapped to the first configuration, ..." To the contrary, Fluegge only describes reversing the order of the levels of the wires which is a necessary consequence of the FPGA structure being discussed. This is different than *N* inputs mapped inverse to *N* outputs. As an illustrative example, Fluegge might route bit 1 of an input, through several levels up, to bit 1 of an output in a first SECTOR and then from bit 1 of an input, down several levels, to bit 1 of an output of a second SECTOR. In a

contrasting illustrative example, the Applicant's claim would cover mapping bit 1 of an input to bit 2 of an output of a first routing portion, and then mapping bit 2 of an input to bit 1 of an output of a second routing portion. Fluegge, in the cited portion or in its entirety, does not address mapping two routing portions inversely from one another.

As such, because the combination of Butts, Cote and Fluegge fails to teach or suggest each and every feature of Applicants' claim 13, withdrawal of the rejection is respectfully requested.

Applicants' claims 14-17, which depend on claim 13, are patentably distinct over the art of record for at least the same reasons as their ultimate base claim and further in view of the novel features recited therein.

Applicants' claim 23 includes similar features as described above with reference to claim 13. As such, Applicants' claim 23 is patentably distinct over the art of record for at least similar reasons as described with respect to claim 13.

Rejections of Claims 18-20 under 35 U.S.C. § 103

Claims 18-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Harris in view of U.S. Pat. No. 5,436,559, hereinafter Takagi. Applicants respectfully traverse.

Harris, and Takagi do not teach each and every limitation of claims 18-20. Assuming, without admitting, that the combination of Harris and Takagi is proper, the combination fails to teach or suggest each and every feature of Applicants' claim 20. The office cites Fig. 1 and column 1, lines 48-58 of Takagi which states:

> FIG. 1 is a conceptional diagram of functional test of a semiconductor device, particularly a semiconductor integrated circuit device. Referring to FIG. 1, a testing apparatus includes a pattern generator 500 for generating a test pattern, a test pattern applying apparatus 501 for receiving the test pattern from pattern generator 500, to convert the received test pattern into logic signals of logical one or logical zero and apply the signals to an input terminal 510 of a device 502 under test, an output pattern discriminating circuit 504 for receiving an output signal from device 502 under test to convert the received output signal into a logic signal, …

Takagi, in the cited portions or in its entirety, fails to provide, as recited by claim 18, "a data processing portion coupled to the first set, the data processing portion configured to provide a

first test pattern to the first set, wherein the first set is configured to provide a second test pattern to test the second set, ..." While Takagi discloses a pattern generator 500 for generating a test pattern, the test pattern applying apparatus 501 only converts the test pattern into logic signals. In other words, the test pattern applying apparatus outputs the same test pattern as the pattern generator 500, but at corresponding particular voltages that are specific to the technology of the integrated circuit under test. One skilled in the art would understand that physical signal conversion of Takagi is very different conceptually from the Applicants' claim which is a logical pattern translation where the first and second test patterns are of the same physical form but conceivably different states.

As such, because the combination of Harris and Takagi fails to teach or suggest each and every feature of Applicants' claim 18, withdrawal of the rejection is respectfully requested.

Applicants' claims 19-20, which depend on claim 18, are patentably distinct over the art of record for at least the same reasons as their ultimate base claim 18 and further in view of the novel features recited therein.

For example, the combination of Harris and Takagi fails to teach claim 20, which recites,

> ... wherein the data processing portion is further configured to provide a third test pattern to the second set, the second set is further configured to provide a fourth test pattern to test the first set, and the first set is further configured to output second data in response to fourth test pattern received from the second set.

The office action cites the same portion of Takagi cited above. This disclosure does not state that the "second set," that is tested by the "first set," is configured to have the "first set" be tested by the "second set." Similarly, as argued for claim 2 above, Harris also does not disclose similar structure.

Rejections of Claim 22 under 35 U.S.C. § 103

Claim 22 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Harris in view of Takagi and Venkatesan . Applicants respectfully traverse.

Harris, Takagi, and Venkatesan do not teach each and every limitation of claim 22. Claim 22, which depend on claim 18, is patentably distinct over the art of record for at least the

same reasons as its base claim and further in view of the novel features recited therein. Further, claim 22, contains similar distinguishable language as claim 1, and is patently distinct from the prior art for at least the same reasons as claim 1.

Accordingly, because the combination of Harris, Takagi, and Venkatesan fails to teach or suggest each and every feature of Applicants' claim 22, withdrawal of the rejection is respectfully requested.

Rejections of Claim 24 under 35 U.S.C. § 103

Claim 24 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 5,903,744, hereinafter Tseng, in view of Harris and Takagi. Applicants respectfully traverse.

Tseng, Harris, and Takagi do not teach each and every limitation of claim 24. Claim 24 recites similar language as claim 2 and claim 20. For the reasons given for those claims, the combination of Harris and Takagi, as alleged in the office action, do not teach the limitation of , "...a first test pattern to the first set to test the second set and a second test pattern to the second set to test the first set." Further, Tseng, as conceded by the office action, also does not teach this limitation.

Accordingly, because the combination of Tseng, Harris, and Takagi fails to teach or suggest each and every feature of Applicants' claim 24, withdrawal of the rejection is respectfully requested.

Rejections of Claim 25 under 35 U.S.C. § 103

Claim 25 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Tseng in view of Butts, Cote, and Fluegge. Applicants respectively traverse.

Tseng, Butts, Cote and Fluegge do not teach each and every limitation of claim 25. Claim 25 contains similar language to claim 13 and 23. For the reasons given for those claims, the combination of Butts, Cote, and Fluegge, as alleged in the office action, does not teach the limitation of , "wherein the second routing portion is configured to map *N* inputs of the second routing portion to *N* outputs of the second routing portion in a second manner inverse to the first

manner, and is configured to output data." Further, Tseng, as conceded by the office action, also does not teach this limitation.

Tseng is not combinable with Butts. Further, one skilled in the art could not combine Tseng with Butts as alleged in the office action to arrive at Applicants' claim 25. Tseng explicitly teaches away from Butts and the claim 25 limitation, "wherein each of the plurality of interconnect boards has an integrated circuit having first and second routing portions and monitoring logic." Tseng states:

> The invention provides a simpler, less-expensive hardware-based emulator. The switching FPGA's used in prior-art emulators are replaced with the wire-wrap interconnection board. Since wire-wrap is much less expensive than FPGA chips, the cost is reduced substantially. Timing delays through the prior-art's switching FPGA's are eliminated, increasing emulation speed. The size of the emulation system is reduced drastically in comparison to cross-bar FPGA emulators. Manufacturing these emulation systems is easier. (Tseng, col. 7, lines 53)

Tseng specifically teaches a wire wrap interconnection board as an alternative to interconnection with active circuitry.

Accordingly, because the combination of Tseng, Butts, Cote and Fluegge fails to teach or suggest each and every feature of Applicants' claim 25, and because Tseng is not combinable with Butts as alleged by the office action, withdrawal of the rejection is respectfully requested.

CONCLUSION

All issues having been addressed, Applicant respectfully submits that the instant application is in condition for allowance, and respectfully solicits prompt notification of the same. However, if for any reason the Examiner believes the application is not in condition for allowance or there are any questions, the Examiner is requested to contact the undersigned at (202) 824-3153.

Respectfully submitted,

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